REMARKS

Claims 1, 3, 5, 6, 8 and 10-13 are all the claims pending in the application. By this Amendment, Applicant amends claims 1, 5, 6, 8, 10, and 12 to further clarify the invention and adds claim 14. Claim 14 is clearly supported throughout the specification.

As preliminary matters, the Examiner has accepted the replacement drawings filed on September 8, 2005.

The Examiner objected to claim 12 for minor informality. Applicant independently amended claim 12 and respectfully requests the Examiner to withdraw this objection because these independent amendments coincidentally overcome the Examiner's objection to claim 12.

Summary of the Office Action

Claims 1, 3, 5, 6, 8 and 10-13 presently stand rejected. Specifically, claims 5, 6, 8, and 12 are rejected under 35 U.S.C. § 112, first paragraph and claims 1, 3, 5, 6, 8, 10, 11, and 13 are rejected under 35 U.S.C. § 102(a).

Claim Rejections under 35 U.S.C. § 112, first paragraph

Claims 5, 6, 8, and 12 are rejected under 35 U.S.C. § 112, first paragraph. Applicant respectfully traverses this rejection in view of the following comments.

Claims 5, 6, and 8 have been amended to recite: "wherein, when disturbances are generated on the trigger signal during the data transmission/reception, the memory start address is not incremented." Applicant respectfully submits that these unique features of claims 5, 6, and 8 are clearly supported throughout the specification.

For example, in the non-limiting embodiment of the present invention, a cycle signal that counts three times the leading edge of the clock to toggle is provided. That is, the secondary board does not shift to the next process until the phase has been toggled. The leading and trailing edges of the trigger, detected in combination with the toggle states of the phase, prevents disturbances generated on the trigger *i.e.*, "the stability of transmission can be implemented...missing data can be reduced" (page 26, lines 6 to 13 of the specification).

Furthermore, the specification discloses that "the leading edge and the trailing edge of the TRG 21 are detected in combination with the toggle states of the PHASE 32. Therefore, in addition to the advantages of the embodiment 1, malfunction in generating the MA 15:0 in the separator 26A of the secondary board can be prevented even if disturbances such as the crosstalk, the reflection, etc. are generated on the TRG 21, and also great deal of continuous data transmission can be accomplished via fewer signal lines safely against the disturbances" (page 39, lines 1 to 8 of the specification). That is, by using the cycle signal and the trigger signal in combination, erroneous count up of the address increment may be prevented even when noise is overlapped on the trigger (Fig. 12; pages 30 and 31 of the specification). That is, the address is not incremented during the time in which the disturbances are generated on the trigger signal.

For at least these exemplary reasons, it is respectfully submitted that the features set forth in claims 5, 6, and 8 are clearly supported throughout the specification. It is appropriate and necessary for the Examiner to withdraw this rejection of claims 5, 6, and 8.

With respect to claim 12, the Examiner alleges that "the trigger signal is toggled only in response to switching state of the cycle signal" is new matter (*see* page 3 of the Office Action).

Applicant respectfully requests the Examiner to withdraw this rejection of claim 12 in view of these self-explanatory claim amendments. The proposed amendment to claim 12 is clearly supported throughout the specification *e.g.*, page 27, lines 17 to 19 of the specification.

Claim Rejections under 35 U.S.C. § 102(a)

Claims 1, 3, 5, 6, 8, 10 11, and 13 are rejected under 35 U.S.C. § 102(a) as being anticipated by Applicant Admitted Prior Art (hereinafter "APA"). Applicant respectfully traverses in view of the following comments.

Claim 1, among a number of unique features, recites: "the cycle signal counts plural times a leading edge of a clock signal of the primary board prior to toggle of the cycle signal." The Examiner alleges that the APA's start address A1:0 discloses the cycle signal as set forth in claim 1 (*see* page 15 of the Office Action).

The APA, however, only discloses the signal A1:0, which indicates the lower two bits of the data transmission bus (page 2 of the specification). That is, the signal A1:0 is used for outputting the lower bits of the address. In the APA, the number of data in the continuous transmission is decided by the number of lower address signal lines A1:0 (page 7 of the specification). The APA, however, fails to disclose or suggest the lower address signal counting plural times the leading edge of a clock of the primary board.

Moreover, the APA fails to disclose or suggest the lower address signal being a toggle signal. The Examiner alleges that A0 in the signal A1:0 is changed from 0 to 1 to 0 and accordingly, the Examiner reasons that the address signal A1:0 is toggled (*see* page 16 of the Office Action). Applicant respectfully disagrees. A0 is a portion of the signal A1:0 and not a

signal as set forth in claim 1. The signal A1:0 indicates the lower bits of the address (page 7 of the specification) and as such is not a toggle signal.

Therefore, "the cycle signal counts plural times a leading edge of a clock signal of the primary board prior to toggle of the cycle signal," as set forth in claim 1 is not taught by the APA, which lacks having the start address signal counting plural times a leading edge of the clock signal of the primary board prior to its toggle. Claims 3 and 11-13 are patentable at least by virtue of their dependency on claim 1.

In addition, dependent claim 12 recites: "the cycle signal is a separate toggle signal having only two states and wherein the trigger signal illustrates write and read timing of the data transmission path." The APA fails to disclose or suggest the start address A1:0 being a separate toggle signal with only two states. The start address A1:0 carries lower bits and as such can assume more than two states. The alleges A0 is a portion of the signal A1:0 and as such is not a separate toggle signal. For at least these additional exemplary reasons, claim 12 patentably distinguishes from the APA.

Dependent claim 13 recites: "the secondary board generates subsequent addresses used in data access based on the start address and wherein the subsequent addresses are generated by the secondary board by incrementing last address used." The Examiner alleges that S233 in Fig. 21 of the APA discloses these unique features of claim 1 (*see* pages 13 to 14 of the Office Action). Applicant respectfully disagrees.

S233 in Fig. 21 of the APA only discloses assigning to the MA 15:0 the transmitted address A15:2 and A1:0. That is, the address MA 15:0 is synthesized from the addresses A15:2

and A1:0 (*see* pages 4 to 5 of the specification). In the APA, however, a subsequent address is not generated. In the APA, the address is simply synthesized from the two transmitted addresses *i.e.*, M1:0 is assigned A1:0 and M15:2 is assigned to A15:2. That is, the APA fails to disclose or suggest the second board generating subsequent address by incrementing the last address used, as required in claim 13. For at least these additional exemplary reasons, claim 13 is patentably distinguishable from the APA.

With respect to independent claims 5, 6, 8, and 10, Applicant amends these claims similar to the amendment made to claim 1. Accordingly, claims 5, 6, 8, and 10 are patentable at least for analogous exemplary reasons.

In addition, claim 5 recites: "when disturbances are generated on the trigger signal during the data transmission/reception, the memory start address is not incremented." The Examiner alleges that during frame deformation (when FRAME is set to H by triggering noise), the secondary board quits the read/write operation and as such meets the unique features of claim 5 (*see* page 16 of the Office Action). Applicant respectfully disagrees.

In particular, this instance of the frame signal being switched to high is inapplicable because the transmission/reception of data is not performed when the frame is switched to high. In the present case, in the APA, the address is changed when the trigger signal is raised, *e.g. see* T43, T44, and so on (*see* page 5 of the specification). Accordingly, the APA does not teach or suggest not incrementing the memory start address during disturbances generated on the trigger signal. In short, the APA fails to teach or suggest when disturbances are generated on the trigger signal during the data transmission/reception, not incrementing the memory start address.

New Claims

In order to provide more varied protection Applicant adds claim 14. Claim 14 is patentable at least by virtue of its dependency on claim 1.

Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly invited to contact the undersigned attorney at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

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